OIPE IAP54
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PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	John Bruno	Examiner:	Nathan W. Ha
Serial No.:	10/064,856	Art Unit:	2814
Filing Date:	August 23, 2002	Docket No.:	00100.02.0038

Title: **INTEGRATED CIRCUIT HAVING MEMORY DISPOSED THEREON AND METHOD OF MAKING THEREOF**

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Commissioner for Patents
P.O. Box 1450
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11/7/06

AFTER FINAL RESPONSE

Dear Sir:

In response to the Final Office Action mailed July 19, 2005, for the above-identified patent application, Applicant responds as follows:

REMARKS

Applicant respectfully traverses and requests reconsideration.

Claims 1, 2, 5-9, and 21-22 stand rejected under 35 U.S.C. §102(e) as being anticipated by Urakawa. If the rejection is maintained, Applicant respectfully requests that the finality of the office action be withdrawn as it does not appear to provide a prima facia §102(e) rejection with respect to claims 8 or 22 since these claims are not mentioned in the §102(e) rejection.

As to claim 1, in the "Response to Arguments" section, the office action also does not address Applicant's remarks regarding the system memory limitation and in particular, the office action fails to point out where the Urakawa reference teaches system memory that is operative to store system instructions that is in electrical communication on the carrier substrate with the information router via electrical leads and wherein the system instructions are stored and